USER MANUAL

# A64-µQ System-on-Module

## 64-bit Quad-core ARM Cortex-A53

featuring the Allwinner A64 application processor

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CHAPTER

# ONE

# INTRODUCTION

**Note:** The latest version of this manual and related resources can always be found on our website at the following address:

https://www.theobroma-systems.com/a64-uq7

This is a PRELIMINARY VERSION of the A64-uQ7 user manual. The hardware description is complete. The software chapter will be added in the next release of this manual.

CHAPTER

TWO

# HARDWARE GUIDE

## 2.1 About this Chapter

This Hardware Guide provides information about the features, connectors and signals available on the A64-µQ7 module.

## 2.2 Qseven Implementation

Qseven has mandatory and optional features. Following table shows the feature set of the A64 µQ7 module compared to the minimum ARM/RISC based and maximum configuration according to the Q7 standard.

| System I/O Interface | Q7 Minimum | A64 µQ7 | Q7 Maximum |
|---|---|---|---|
| PCI Express lanes | 0 | 0 | 4 |
| Serial ATA channels | 0 | 0 | 2 |
| USB 2.0 ports | 3 | 7 | 8 |
| USB 3.0 ports | 0 | 0 | 2 |
| LVDS channels | 0 | 0 | 2 |
| Embedded DisplayPort | 0 | 0 | 1 |
| HDMI | 0 | 1 | 1 |
| High Definition Audio / AC‘97 / I2S | 0 | 1 | 1 |
| Ethernet 10/100/Gigabit | 0 | 1x Gigabit | 1x Gigabit |
| UART | 0 | 1 | 1 |
| GPIO | 0 | 8 | 8 |
| Secure Digital I/O | 0 | 1 | 1 |
| System Management Bus | 0 | 1 | 1 |
| $I^2C$ Bus | 1 | 1 | 3 |
| SPI Bus | 0 | 1 | 1 |
| CAN Bus | 0 | 1 | 1 |
| Watchdog Trigger | 1 | 1 | 1 |
| Power Button | 1 | 1 | 1 |
| Power Good | 1 | 1 | 1 |
| Reset Button | 1 | 1 | 1 |
| LID Button | 0 | 1 | 1 |
| Sleep Button | 0 | 1 | 1 |
| Suspend To RAM (S3 mode) | 0 | 1 | 1 |
| Wake | 0 | 1 | 1 |
| Battery low alarm | 0 | 1 | 1 |
| Thermal control | 0 | 1 | 1 |
| FAN control | 0 | 1 | 1 |

**Note:** The A64 µQ7 module is available in different variants. This document describes the maximum configuration. For details about orderable variants please refer to the the order-code document.

## 2.3 Connector Description

The following table shows the signals on the edge connector of the A64 µQ7 module.

Empty cells are not connected (NC) pins.

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | GBE_MDI3- | 4 | GBE_MDI2- |
| 5 | GBE_MDI3+ | 6 | GBE_MDI2+ |
| 7 | GBE_LINK100# | 8 | GBE_LINK1000# |
| 9 | GBE_MDI1- | 10 | GBE_MDIO0- |
| 11 | GBE_MDI1+ | 12 | GBE_MDIO0+ |
| 13 | GBE_LINK# | 14 | GBE_ACT# |
| 15 | | 16 | SUS_S5# |
| 17 | WAKE# | 18 | SUS_S3# |
| 19 | GP0 | 20 | PWRBTN# |
| 21 | SLP_BTN# | 22 | LID_BTN# |
| 23 | GND | 24 | GND |
| 25 | GND | 26 | PWGIN |
| 27 | BATLOW# | 28 | RSTBTN# |
| 29 | | 30 | |
| 31 | | 32 | |
| 33 | | | 34 GND |
| 35 | | 36 | |
| 37 | | 38 | |
| 39 | GND | 40 | GND |
| 41 | BIOS_DISABLE# / BOOT_ALT# | 42 | SDIO_CLK# |
| 43 | SDIO_CD# | 44 | SDIO_LED |
| 45 | SDIO_CMD | 46 | SDIO_WP |
| 47 | SDIO_PWR# | 48 | SDIO_DAT1 |
| 49 | SDIO_DAT0 | 50 | SDIO_DAT3 |
| 51 | SDIO_DAT2 | 52 | |
| 53 | | 54 | |
| 55 | | 56 | USB_OTG_PEN |
| 57 | GND | 58 | GND |
| 59 | I2S_WS | 60 | SMB_CLK / GP1_I2C_CLK |
| 61 | I2S_RST# | 62 | SMB_DAT / GP1_I2C_DAT |
| 63 | I2S_CLK | 64 | SMB_ALERT# |
| 65 | I2S_SDI | 66 | GP0_I2C_CLK |
| 67 | I2S_SDO | 68 | GP0_I2C_DAT |
| 69 | THRM# | 70 | WDTRIG# |
| 71 | THRMTRIP# | 72 | WDOUT |

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| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 73 | GND | 74 | GND |
| 75 | | 76 | USB_P6- |
| 77 | | 78 | USB_P6+ |
| 79 | USB_6_7_OC# | 80 | USB_4_5_OC# |
| 81 | USB_P5+ | 82 | USB_P4- |
| 83 | USB_P5- | 84 | USB_P4+ |
| 85 | USB_2_3_OC# | 86 | USB_0_1_OC# |
| 87 | USB_P3- | 88 | USB_P2- |
| 89 | USB_P3+ | 90 | USB_P2+ |
| 91 | USB_CC | 92 | USB_ID |
| 93 | USB_P1- | 94 | USB_P0- |
| 95 | USB_P1+ | 96 | USB_P0+ |
| 97 | GND | 98 | GND |
| 99 | | 100 | DSI_D0+ |
| 101 | | 102 | DSI_D0- |
| 103 | | 104 | DSI_D1+ |
| 105 | | 106 | DSI_D1- |
| 107 | | 108 | DSI_D2+ |
| 109 | | 110 | DSI_D2- |
| 111 | LVDS_PPEN | 112 | LVDS_BLEN |
| 113 | | 114 | DSI_D3+ |
| 115 | | 116 | DSI_D3- |
| 117 | GND | 118 | GND |
| 119 | | 120 | DSI_C+ |
| 121 | | 122 | DSI_C- |
| 123 | LVDS_BLT_CTRL / GP_PWM_OUT0 | 124 | GP_1-Wire_Bus |
| 125 | GP2_I2C_DAT / LVDS_DID_DAT | 126 | LVDS_BLC_DAT / eDP0_HPD# |
| 127 | GP2_I2C_CLK / LVDS_DID_CLK | 128 | LVDS_BLC_CLK |
| 129 | CAN0_TX | 130 | CAN0_RX |
| 131 | TMDS_CLK+ | 132 | |
| 133 | TMDS_CLK- | 134 | |
| 135 | GND | 136 | GND |
| 137 | TMDS_LANE1+ | 138 | |
| 139 | TMDS_LANE1- | 140 | |
| 141 | GND | 142 | GND |

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| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 143 | TMDS_LANE0+ | 144 | |
| 145 | TMDS_LANE0- | 146 | |
| 147 | GND | 148 | GND |
| 149 | TMDS_LANE2+ | 150 | HDMI_CTRL_DAT |
| 151 | TMDS_LANE2- | 152 | HDMI_CTRL_CLK |
| 153 | DP_HDMI_HPD# | 154 | |
| 155 | | 156 | |
| 157 | | 158 | |
| 159 | GND | 160 | GND |
| 161 | | 162 | |
| 163 | | 164 | |
| 165 | GND | 166 | GND |
| 167 | | 168 | |
| 169 | | 170 | |
| 171 | UART0_TX | 172 | UART0_RTS# |
| 173 | | 174 | |
| 175 | | 176 | |
| 177 | UART0_RX | 178 | UART0_CTS# |
| 179 | | 180 | |
| 181 | | 182 | |
| 183 | GND | 184 | GND |
| 185 | GPIO0 | 186 | GPIO1 |
| 187 | GPIO2 | 188 | GPIO3 |
| 189 | GPIO4 | 190 | GPIO5 |
| 191 | GPIO6 | 192 | GPIO7 |
| 193 | VCC_BAT | 194 | SPKR / GP_PWM_OUT2 |
| 195 | FAN_TACHOIN / GP_TIMER_IN | 196 | FAN_PWMOUT / GP_PWM_OUT1 |
| 197 | GND | 198 | GND |
| 199 | SPI_MOSI | 200 | SPI_CS0# |
| 201 | SPI_MISO | 202 | SPI_CS1# |
| 203 | SPI_SCK | 204 | |
| 205 | VCC_5V_SB | 206 | VCC_5V_SB |
| 207 | JTAG_TCK | 208 | JTAG_TDI |
| 209 | JTAG_TDO | 210 | JTAG_TMS |
| 211 | | 212 | |

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| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 213 | | 214 | |
| 215 | | 216 | |
| 217 | | 218 | |
| 219 | VCC | 220 | VCC |
| 221 | VCC | 222 | VCC |
| 223 | VCC | 224 | VCC |
| 225 | VCC | 226 | VCC |
| 227 | VCC | 228 | VCC |
| 229 | VCC | 230 | VCC |

## 2.4 Signal Description

### 2.4.1 Ethernet

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| GBE_MDI[0:3]+<br>GBE_MDI[0:3]- | I/O | Analog | Gigabit Ethernet Controller: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit/sec modes |
| GBE_ACT# | OC | 3.3V | Gigabit Ethernet Controller activity indicator, active low |
| GBE_LINK# | OC | 3.3V | Gigabit Ethernet Controller link indicator, active low |
| GBE_LINK100# | OC | 3.3V | Internaly connected to GBE_LINK# |
| GBE_LINK1000# | OC | 3.3V | Internaly connected to GBE_LINK# |
| GBE_CTREF | REF | Analog | Center Tap Voltage |

### 2.4.2 USB

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| USB_P[0:6]+<br>USB_P[0:6]- | I/O | USB | Universal Serial Bus Port 0 to 6 differential pairs |
| USB_0_1_OC# | I | 3.3V | Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1 |
| USB_2_3_OC# | I | 3.3V | Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 2 and 3 |
| USB_6_7_OC# | I | 3.3V | Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 6 and 7 |
| USB_ID | I | 3.3V | Configures the mode of the USB Port 1. If the signal is `active high` the Port will be configured as USB Client |
| USB_VBUS | I | 5.0V | USB VBUS pin, 5V tolerant |
| USB_OTG_PEN | O | 3.3V | USB Power enable for OTG port USB 1 |

### 2.4.3 SDIO

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| SDIO_CD# | I | 3.3V | SDIO Card Detect. This signal indicates when a SDIO/MMC card is present |
| SDIO_CLK | O | 3.3V | SDIO Clock |
| SDIO_CMD | I/O | 3.3V | SDIO Command/Response |
| SDIO_LED | O | 3.3V | SDIO LED. Used to drive an external LED to indicate transfers on the bus |
| SDIO_WP | I | 3.3V | SDIO Write Protect |
| SDIO_PWR# | O | 3.3V | SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device |
| SDIO_DAT0-4 | I/O | 3.3V | SDIO Data lines |

### 2.4.4 I2C

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| Q7_I2C_CLK | O | 3.3V | I2C bus clock line connected to A64, STM32, Kerkey accelerometer, humidity temperature sensor |
| Q7_I2C_DAT | I/O | 3.3V | I2C bus data line connected to A64, STM32, Kerkey accelerometer, humidity temperature sensor |
| LVDS_DID_CLK /GP2_I2C_CLK | O | 3.3V | I2C bus clock line connected to A64 |
| LVDS_DID_DAT /GP2_I2C_DAT | I/O | 3.3V | I2C bus data line connected to A64 |
| SMB_CLK GP1_I2C_CLK | O | 3.3V | Clock line of System Management Bus. Alternate function I2C Bus clock line |
| SMB_DAT GP1_I2C_DAT | I/O | 3.3V | Data line of System Management Bus. Alternate function I2C Bus data line |

### 2.4.5 I2S

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| I2S_RST# | O | 3.3V | I2S Codec Reset |
| I2S_WS | O | 3.3V | I2S Word Select |
| I2S_CLK | O | 3.3V | I2S Serial Data Clock |
| I2S_SDO | O | 3.3V | I2S Serial Data Output |
| I2S_SDI | I | 3.3V | I2S Serial Data Input |

### 2.4.6 DSI

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| DSI_D[0:3]+ DSI_D[0:3]- | O | DSI | DSI channel differential pair 0, 1, 2, 3 |
| DSI_C+ DSI_C- | O | DSI | DSI channel differential pair clock lines |
| LVDS_PPEN | O | 3.3V | Controls panel power enable |
| LVDS_BLEN | O | 3.3V | Controls panel backlight enable |
| LVDS_BLT_CTRL /GP_PWM_OUT0 | O | 3.3V | Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output |

### 2.4.7 HDMI

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| TMDS_CLK+ TMDS_CLK- | O | TMDS | TMDS differential pair clock lines |
| TMDS_LANE[0:2]+ TMDS_LANE[0:2]- | O | TMDS | TMDS differential pair lanes 0, 1, 2 |
| HDMI_CTRL_CLK | O | 3.3V | DDC based control signal (clock) for HDMI device |
| HDMI_CTRL_DAT | I/O | 3.3V | DDC based control signal (data) for HDMI device |
| HDMI_HPD# | I | 3.3V | Hot plug detection signal |

### 2.4.8 GPIO

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| GPIO[0-7] | I/O | 3.3V | General purpose inputs/outputs 0 to7 |

### 2.4.9 CAN

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| CAN0_TX | O | 3.3V | CAN (Controller Area Network) TX output for CAN Bus channel 0 |
| CAN0_RX | I | 3.3V | CAN (Controller Area Network) RX inpufor CAN Bus channel 0 |

### 2.4.10 SPI

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| SPI_MOSI | O | 3.3V | Master serial output/Slave serial input signal |
| SPI_MISO | I | 3.3V | Master serial input/Slave serial output signal |
| SPI_SCK | O | 3.3V | SPI clock output |
| SPI_CS0# | O | 3.3V | SPI chip select 0 output |
| SPI_CS1# | O | 3.3V | SPI chip select 1 output (used when two devices are connected) |

### 2.4.11 UART

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| UART0_TX | O | 3.3V | Serial data transmit |
| UART0_RX | I | 3.3V | Serial data recieve |
| UART0_CTS# | I | 3.3V | Handshake signal: ready to send data |
| UART0_RTS# | O | 3.3V | Handshake signal: ready to receive data |

### 2.4.12 JTAG

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| JTAG_CK | I | 3.3V | Test clock |
| JTAG_DO | O | 3.3V | Test data out |
| JTAG_DI | I | 3.3V | Test data in |
| JTAG_MS | I | 3.3V | Test mode select |

### 2.4.13 Misc

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| WDTRIG# | I | 3.3V | Watchdog trigger signal |
| WDOUT | O | 3.3V | Watchdog event indicator |
| SMB_CLK<br>GP1_I2C_CLK | O | 3.3V | Clock line of System Management Bus. Alternate function I2C Bus clock line |
| SMB_DAT<br>GP1_I2C_DAT | I/O | 3.3V | Data line of System Management Bus. Alternate function I2C Bus data line |
| SMB_ALERT# | I | 3.3V | System Management Bus Alert input |
| SPKR<br>GP_PWM_OUT2 | O | 3.3V | Audio enunciator output. Alternate function general purpose PWM output |
| Q7_SATA0_TX_N | O | 3V | Headphone analog output left |
| Q7_SATA0_TX_P | O | 3V | Headphone analog output right |
| BIOS_DISABLE#<br>/BOOT_ALT# | I | 3.3V | Disables the onboard bootloader and uses the one the SD card instead. If no bootloader is available on the SD card it falls back to USB recovery mode |
| GP_1-Wire_Bus | I/O | 3.3V | General Purpose 1-Wire bus interface |
| THRM# | I | 3.3V | Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling |
| THRMTRIP# | O | 3.3V | Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off) |
| FAN_PWMOUT<br>/GP_PWM_OUT1 | O | 3.3V | PWM output for fan speed control. Alternate function general purpose PWM output. Function based on microcontroller firmware |
| FAN_TACHOIN<br>/GP_TIMER_IN | I | 3.3V | Fan tachometer input. Alternate function general purpose timer input. Function based on microcontroller firmware |

### 2.4.14 Power Managment

| Signal | Type | Signal Level | Description |
|---|---|---|---|
| RSTBTN# | I | 3.3V | Reset button input. An active low signal resets the module |
| BATLOW# | I | 3.3V | Battery low input |
| WAKE# | I | 3.3V | External system wake event. An active low signal wakes the module from a sleep state |
| SUS_S3# | O | 3.3V | Indicated that the system is in suspend to ram (S3) |
| SUS_S5# | O | 3.3V | Indicated that the system is in soft-off state (S5) |
| SLP_BTN# | I | 3.3V | Sleep button. Signals the system with an falling edge to transition into sleep or wake from a sleep state |
| LID_BTN# | I | 3.3V | LID button. Low active signal to detect a LID switch to transition into sleep or wake from a sleep state |

### 2.4.15 Power

| Signal | Nominal Input | Description |
|---|---|---|
| VCC | 5V | Main supply for the module |
| VCC_5V_SB | 5V | Additional supply rail for standby functionality. If standby functionality is not needed connect to VCC |
| VCC_RTC | 3V | Backup supply for the RTC. If not used it can be left unconnected |

## 2.5 On-board Devices

### 2.5.1 Power-Manager

The X-Powers AXP803 is connected to the CPU via RSB and an interrupt line:

| AXP Pin | Function | CPU Pin |
|---|---|---|
| 47 | SCL | PL0 |
| 48 | SDA | PL1 |
| 61 | IRQ | NMI (ball G18) |

### 2.5.2 DDR3

- 1GB of DDR3 RAM

### 2.5.3 eMMC

- eMMC connected through the 8-bit wide SDIO interface SDC2 on the CPU.

| Signal | CPU Pin | Linux GPIO # |
|---|---|---|
| RESET | PC16 | 80 |

### 2.5.4 NOR

- 1024 kiB serial NOR flash
- Connected to the CPU via SPI0:

| Signal | CPU Pin |
|---|---|
| CLK | PC2 |
| MOSI | PC0 |
| MISO | PC1 |
| CS | PC3 |

### 2.5.5 Cortex-M0

The on-board microcontroller provides additional features to the CPU, exposed via I2C and USB. It emulates standard ICs and does not need custom drivers in Linux.

| Feature | CPU Connection | Emulated IC | Qseven Pins |
|---|---|---|---|
| RTC | I2C | ISL1208 | none |
| Temperature sensor and fan controller | I2C | AMC6821 | FAN_TACHOIN, FAN_PWMOUT |
| CAN | USB | | CAN0_TX, CAN0_RX |

The microcontroller can be flashed from the CPU by taking it into DFU mode (USB recovery). Pull BOOT0 high and cycle reset (GPIOs listed below). The microcontroller will appear as a new USB device in Linux.

| Function | CPU Pin | Linux GPIO # |
|---|---|---|
| NRST | PE0 | 128 |
| BOOT0 | PE1 | 129 |

### 2.5.6 USB

The Genesys Logic, Inc. GL852G provides two or six additional USB 2.0 high-speed ports, depending on slected placement option. The routing of Qseven signals to CPU and/or hub ports depending on the placement option is shown below.

Option with no USB HUB placed:

| Qseven Port # | Speed | Connected to | Hub Port # | Notes |
|---|---|---|---|---|
| USB_P0 | USB 2.0 Hi-Speed | CPU | 1 | |
| USB_P1 | USB 2.0 Hi-Speed | CPU | 0 | USB 2.0 OTG Port |

Option with one USB HUB (HUB0) placed:

| Qseven Port # | Speed | Connected to | Hub Port # | Notes |
|---|---|---|---|---|
| USB_P0 | USB 2.0 Hi-Speed | HUB0 | 1 | |
| USB_P1 | USB 2.0 Hi-Speed | CPU | 0 | USB 2.0 OTG Port |
| USB_P2 | USB 2.0 Hi-Speed | HUB0 | 4 | |
| USB_P3 | USB 2.0 Hi-Speed | Hub0 | 3 | |

Option with two USBs (HUB0 and HUB1) placed:

| Qseven Port # | Speed | Connected to | Hub Port # | Notes |
|---|---|---|---|---|
| USB_P0 | USB 2.0 Hi-Speed | HUB0 | 1 | |
| USB_P1 | USB 2.0 Hi-Speed | CPU | 0 | USB 2.0 OTG Port |
| USB_P2 | USB 2.0 Hi-Speed | HUB1 | 1 | |
| USB_P3 | USB 2.0 Hi-Speed | Hub0 | 3 | |
| USB_P4 | USB 2.0 Hi-Speed | Hub1 | 2 | |
| USB_P5 | USB 2.0 Hi-Speed | Hub1 | 3 | |
| USB_P6 | USB 2.0 Hi-Speed | Hub1 | 4 | |

The routing of the reset signal is shown below.

| Hub signal | CPU Pin | Linux GPIO # |
|---|---|---|
| HUB_RESET_0 | PG9 | |
| HUB_RESET_1 | PE4 | |

### 2.5.7 Ethernet-PHY

The Micrel KSZ9031RNX is connected to the CPU via RGMII and MDIO. Further connections are shown below.

| PHY signal | Connected to | Linux GPIO # |
|---|---|---|
| RESET | CPU pin PD24 | |
| MDIO | CPU pin PD23 | |
| MDC | CPU pin PD22 | |
| LED1 | Qseven GBE_LINK1000 and GBE_LINK100 and GBE_LINK (tied together) | |
| LED2 | Qseven GBE_ACT | |

### 2.5.8 Testpoints

| Testpoint | Connected to |
|---|---|
| TP1 | STM32 USART2 RX |
| TP2 | STM32 USART2 TX |

## 2.6 Electrical Specification

### 2.6.1 Power Supply

The power supply requirements are listed in the table below and are identical to the Qseven specification.

If the base board does not provide standby power, VCC_5V_SB must be tied to VCC.

| Rail | Description | Nominal voltage | Tolerance |
|---|---|---|---|
| VCC | Main power supply | 5V | 4.75 ... 5.25V |
| VCC_5V_SB | Standby power supply | 5V | 4.75 ... 5.25V |
| VCC_RTC | Backup battery | 3V | 2.4 ... 3.3V |

## 2.7 Mechanical Specification

### 2.7.1 Module Dimensions

The mechanical dimensions of the module are shown below.

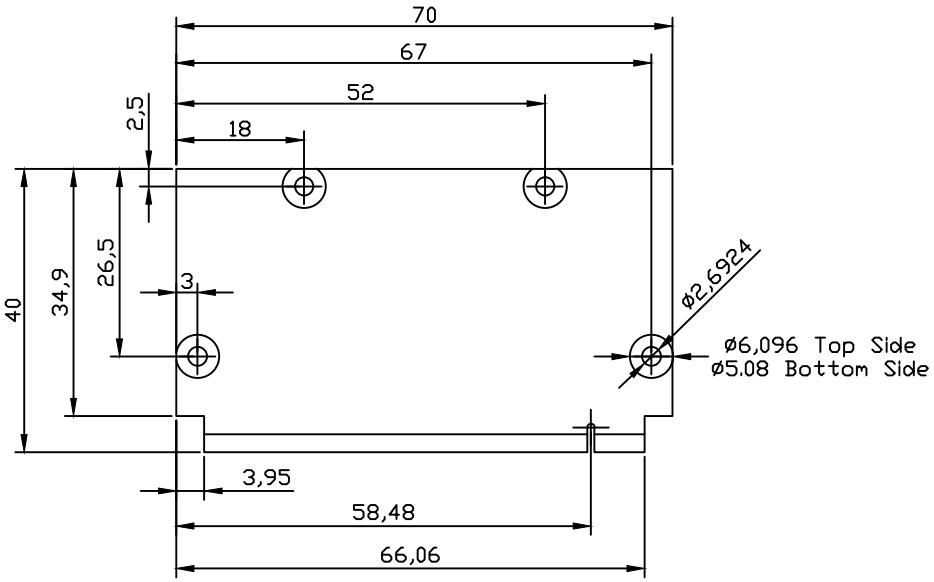


Fig. 2.1: Module dimensions (all values in mm)

CHAPTER

THREE

# ACRONYMS AND ABBREVIATIONS

**ARM** Advanced RISC Machine

**CAN** Controller Area Network

**GCC** GNU Compiler Collection

**HDMI** High Definition Multimedia Interface

**I2C** Inter-Integrated Circuit Bus

**JTAG** Joint Test Action Group

**NTP** Network Time Protocol

**SATA** Serial ATA

**SPI** Serial Parallel Interface

**U-Boot** Universal Bootloader

**USB** Universal Serial Bus

CHAPTER

FOUR

# REVISION HISTORY

| Date | Revision | Changes |
|---|---|---|
| May 4, 2017 | v0.2.1 | Typography: improve legitibity of numbers |
| Dec 15, 2016 | v0.2 | Public release of the preliminary version |